SUMMER SCHOOL 2023 - 1ST HIPO CONFERENCE IN ELECTRIC DRIVES TECHNOLOGY LABORATORY

Parasitic inductance in power electronic circuits

Applied to the Intermediate Circuit of a Multimegawatt Medium-Voltage Neutral-Point-Clamped Inverter

Aleksi Mattsson - LUT University

ABOUT THE AUTHOR

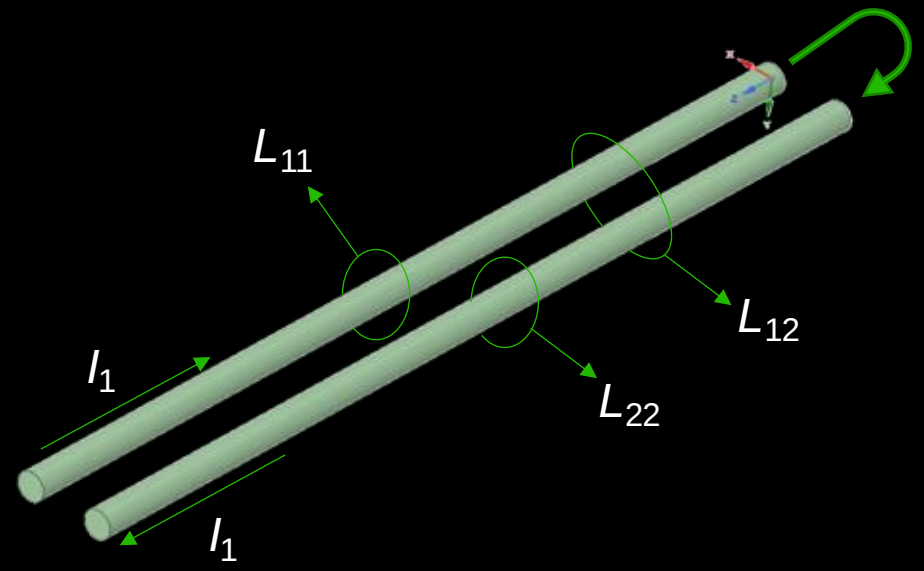
- D.Sc. Aleksi Mattsson
  - Research background
    - Applications
      - Power electronic solutions in low-voltage DC distribution (±750/1500 VDC)
      - Medium-voltage converters
      - Power electronics in water purification
      - Electric power trains of hybrid working machines
    - Analyses
      - Life-cycle cost analysis and optimization of power electronics
      - Finite-element analysis of power electronics (e.g. commutation loop inductances, thermal aspects)

BASICS OF PARASITIC INDUCTANCE

- What is self and mutual inductance?
- What is loop inductance?
- Why loop inductance matters in power electronics design?

BASICS OF PARASITIC INDUCTANCE

- Self inductance
  - Determined by the materials and geometry of each individual conductor
- Mutual inductance
  - Determined by the magnetic fields from each conductor
  - Mutual inductance is affected by the distance between the two conductors
- Loop inductance
  - Inductance of the whole current path when it forms a loop
  - Includes both the self partial and mutual partial inductances
  - $L_{loop}=L_{11}+L_{22}-2L_{12}$
    - If the current in both conductors is flowing in opposite directions, the loop inductance is lower than the sum of the self partial inductances of both conductors



BASICS OF PARASITIC INDUCTANCE

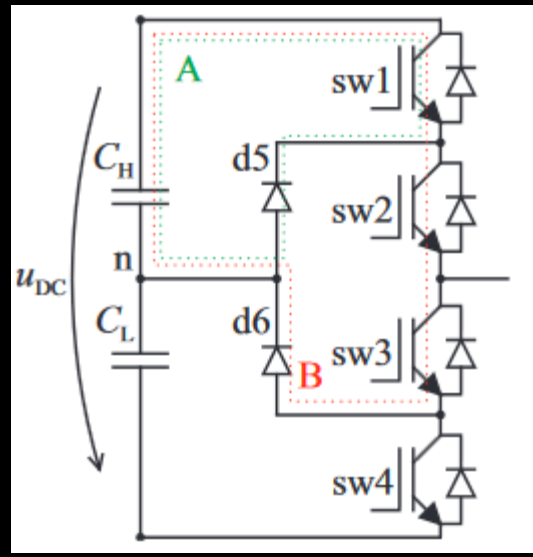
- Why loop inductance matters in power electronics design?
  - Power electronic converters typically include a semiconductor bridge that is connected to capacitors (e.g an intermediate DC link)
  - The connection between the semiconductors and the capacitors has both self partial and mutual partial inductance and forms the loop inductance of the circuit
  - When the semiconductor switch in the current loop is turned off and depending on the current di/dt and the loop inductance value, a high overvoltage spike can be generated due to the stored energy in the loop inductance according to $v = L(di/dt)$
  - Therefore, we want to minimize the loop inductance or otherwise it may become necessary to reduce the di/dt value which can lead to increased switching losses as the semiconductor switch is turned off more slowly and the time in which current and voltage overlap is increased
  - If the overvoltage spike is not maintained below the breakdown voltage of the semiconductor, it will most likely be destroyed

PARASITIC INDUCTANCE IN POWER ELECTRONICS

- Applied to the Intermediate Circuit of a Multimegawatt Medium-Voltage Neutral-Point-Clamped Inverter
  - The layout of the intermediate circuit of a medium-voltage neutral-point-clamped inverter is analysed
  - The placement, orientation and to some extent the number of the DC link capacitors is considered
  - Commutation loop inductances of seven alternative laminated DC link busbar designs are compared against each other.
  - The comparison is carried out by finite element analysis using the Ansys Q3D Extractor and Simplorer circuit simulator.
  - Finally, a prototype of the phase-leg is built and measured to verify the simulation results
  - Our industrial partner does now wish to disclose the full layout of the phase-leg so unfortunately detailed images of the completed phase-leg are not provided

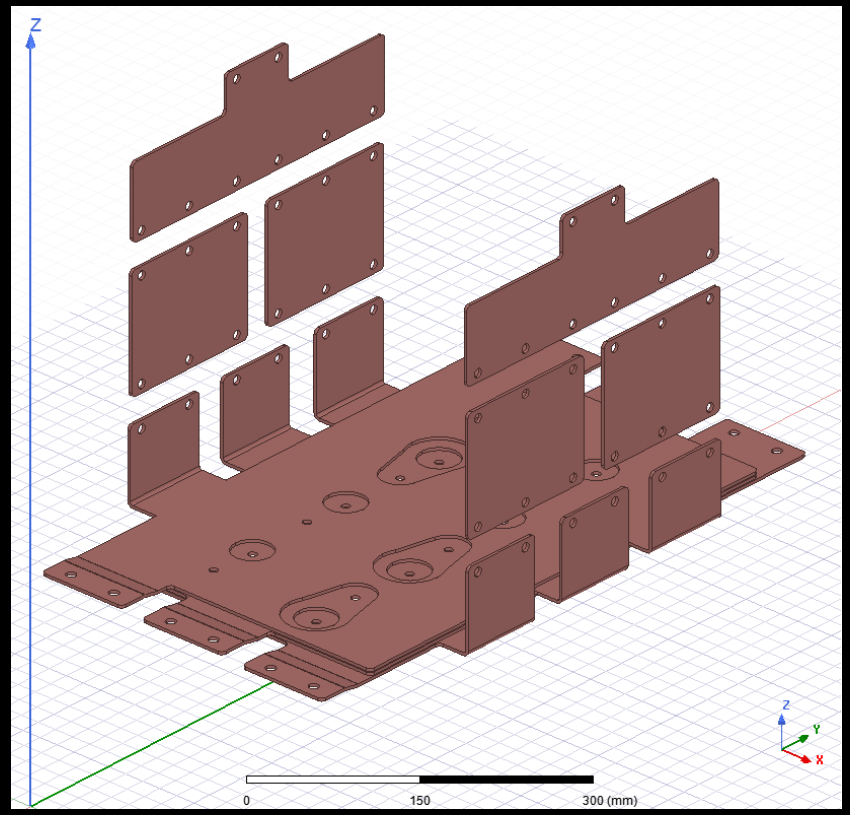
COMMUTATION LOOPS

- The NPC bridge consist of two different types of commutation loops
- The short (A) and long (B) commutation loops of the NPC bridge are shown in the image



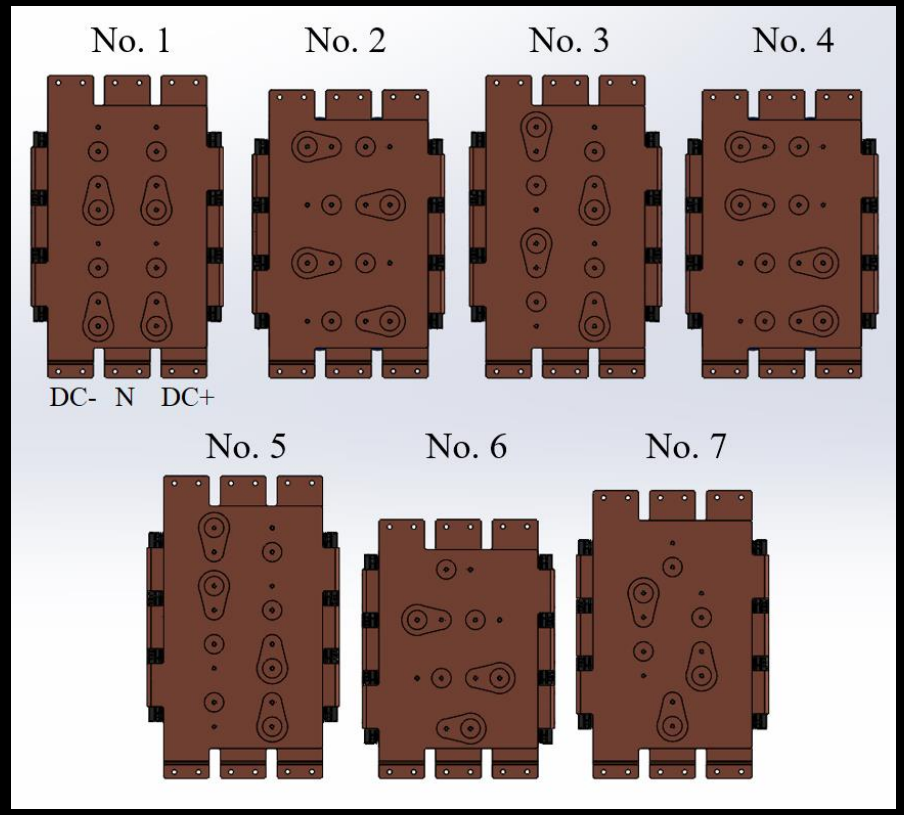
BASE GEOMETRY OF THE PHASE LEG

- Two phase legs in a mirrored configuration connected to a single intermediate circuit
- Possible to implement different combinations of AC-DC and DC-AC conversions



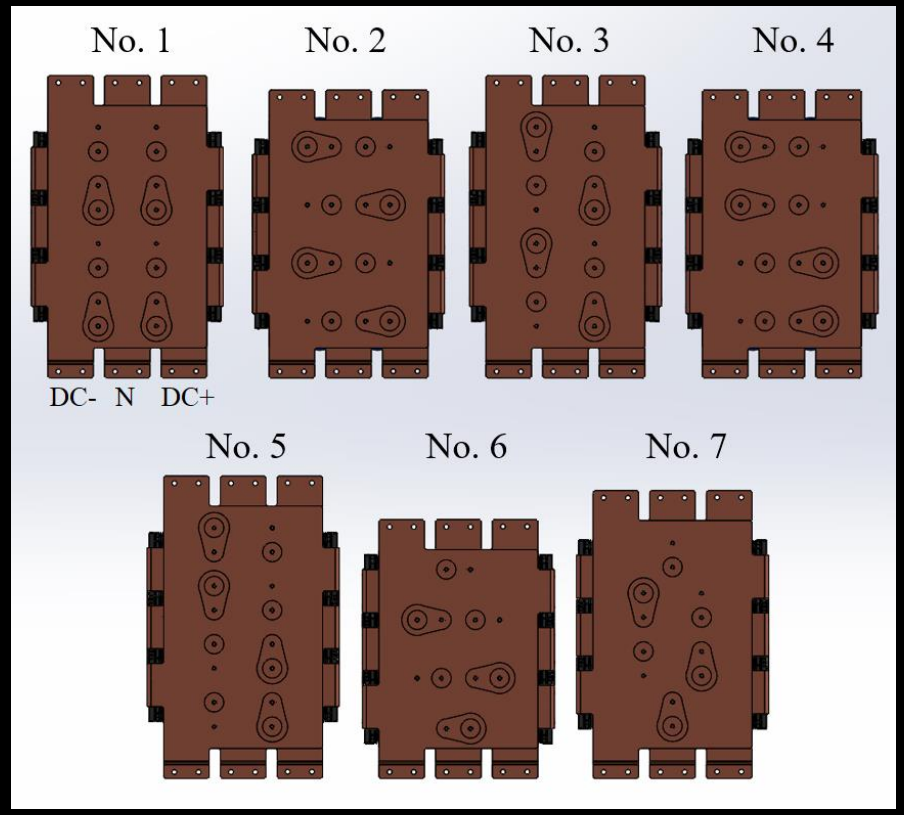
INTERMEDIATE CIRCUIT VARIANTS

- Seven different layouts were created by altering either the placement, number, or orientation of the DC link capacitors
- All layouts utilize a laminated structure
- The neutral layer is placed between the DC+ and DC- layers
- 0.35 mm thick mylar foil is used as insulators between the DC+, N, and DC- busbars



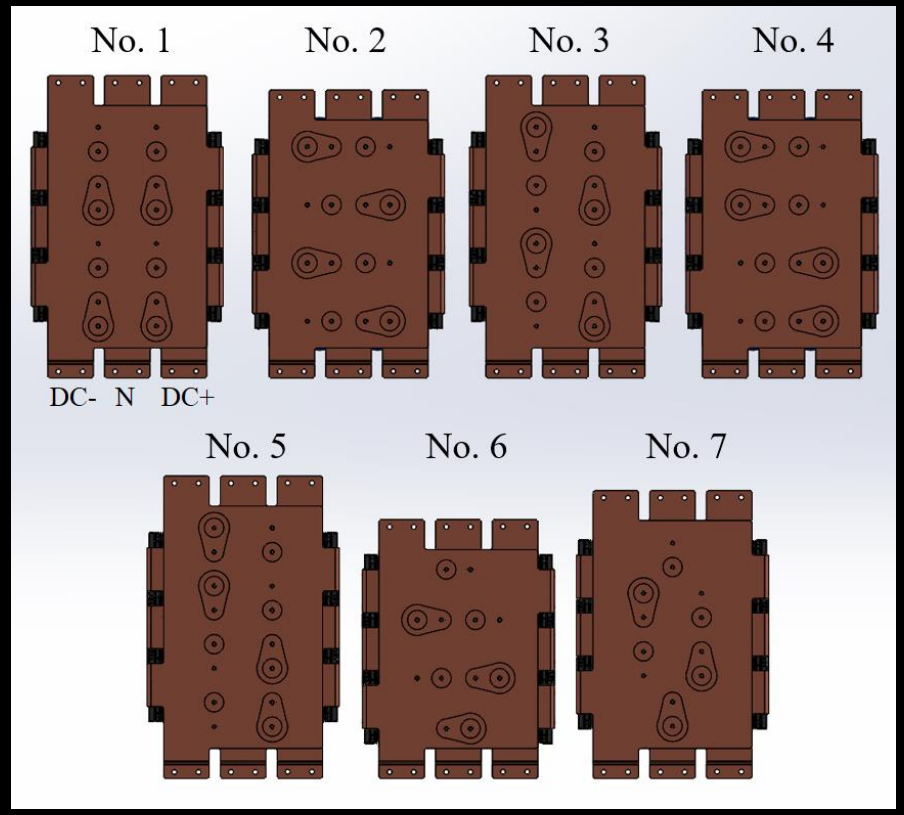
INTERMEDIATE CIRCUIT VARIANTS

- As can be seen in the figure, the number of the DC link capacitors is either six or eight.
- The capacitors are also rotated in some of the layouts to orient the capacitor terminals either parallel to the phase-leg connections or in a 90-degree angle in relation to the phase-leg connections.



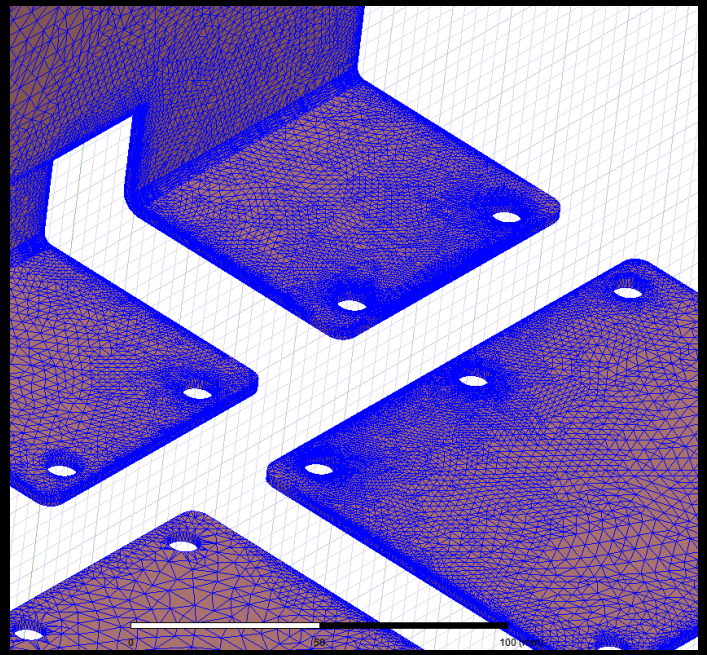
INTERMEDIATE CIRCUIT VARIANTS

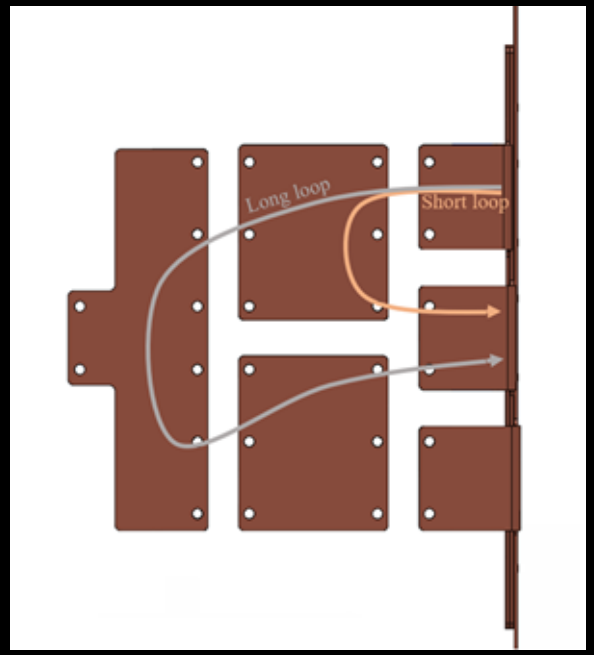
- In layouts 1, 3, and 5 the placement of the capacitors connected to either DC+ or DC- is also altered.
- The intermediate circuit is designed to be connected to two phase-leg modules that are in a mirrored configuration in relation to each other
- Layouts 1, 6, and 7 do not retain symmetry between the commutation loops.



SIMULATION

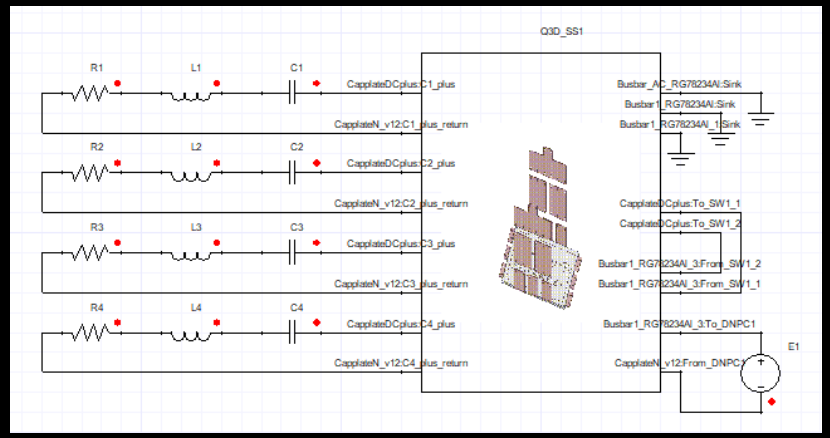
- The simulation was carried out using the Ansys Q3D Extractor and Ansys Simplorer circuit simulator
- An example of the Q3D mesh is shown in the left image
- Commutation loops in relation to the busbars can be seen in the right image

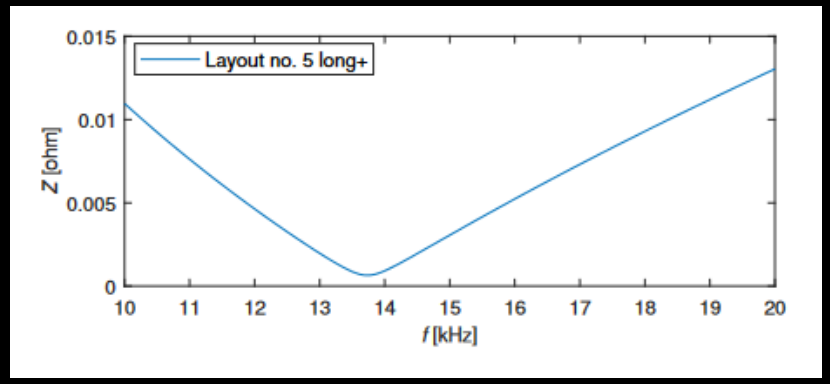




SIMULATION

- RLCG matrices were generated from the Q3D results to enable circuit simulation
- Capacitors were modeled using RLC circuits with parameters R = 0.98 mΩ, L = 60 nH, and C = 170 µF
- The loop inductance can be calculated from the impedance curve





LOOP INDUCTANCES FOR ALL LAYOUTS

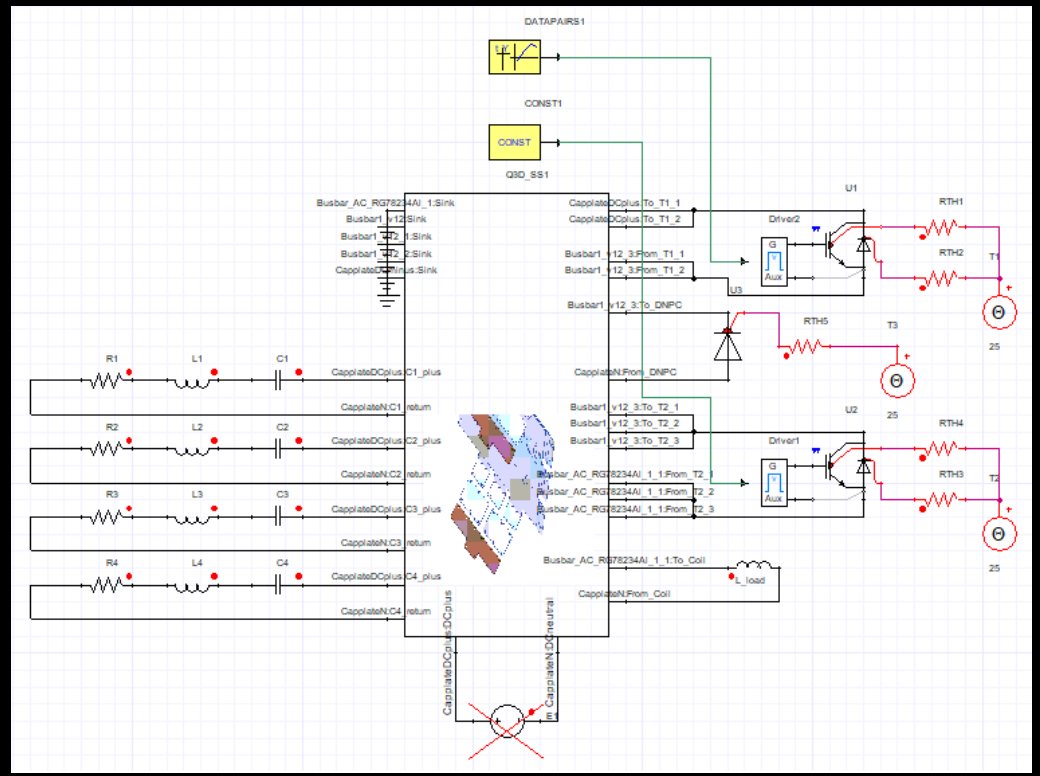
- Differences were smaller than expected
- Layouts 1, 4, and 5 have the lowest loop inductance values but the differences are minor
- Layout 5 was selected for prototyping to verify the simulation results

TABLE I
LOOP INDUCTANCES FOR ALL OF THE SEVEN ANALYSED INTERMEDIATE CIRCUIT DESIGNS.

Comm. loop	Layout number and inductance value in [nH]						
	No.1	No.2	No.3	No.4	No.5	No.6	No.7
DC+ short	82.0	83.3	83.3	82.3	82.3	88.1	87.1
DC- short	83.3	84.5	84.6	83.6	83.6	89.5	88.4
DC+ long	130.7	132.8	132.6	131.4	131.7	137.3	136.3
DC- long	133.2	134.0	134.0	132.8	132.9	138.6	137.6

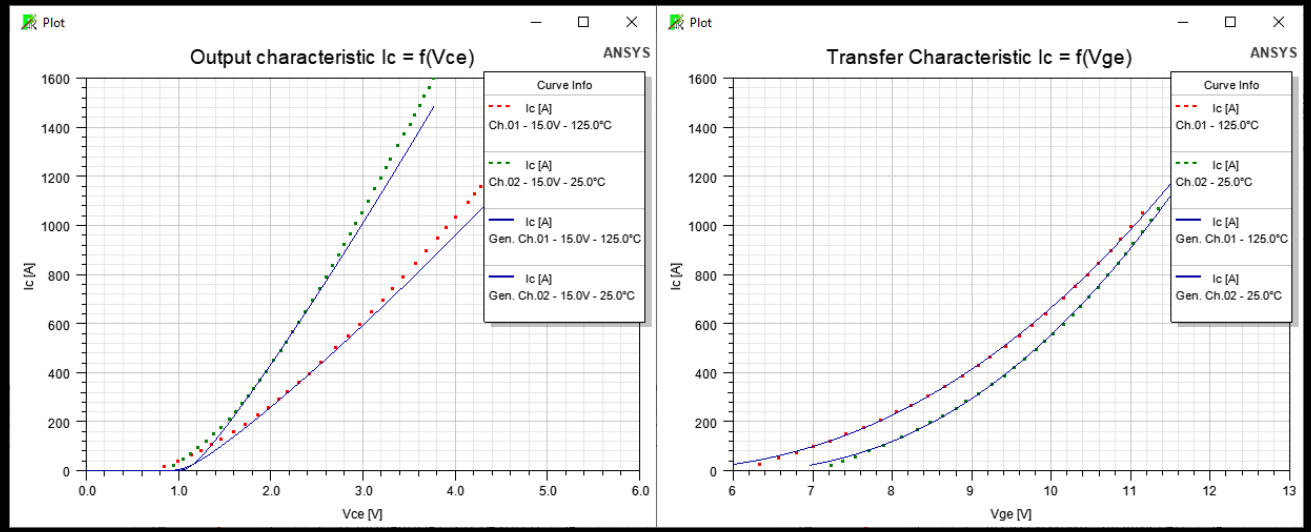
SWITCHING CHARACTERISTICS

- A DPT circuit was implemented in Ansys Simplorer to analyze the switching characteristics
- Semiconductor models include the characteristics of the IGBT modules along with the module parasitic inductance



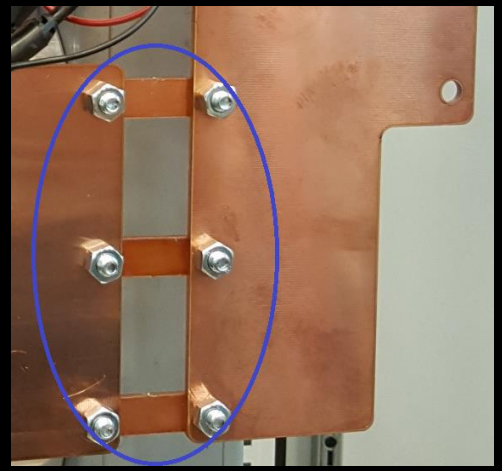
SEMICONDUCTOR MODEL

- Curves from the datasheet are read into the “Characterize device” tool
- Semiconductor parameters are fitted against the input data to create a spice model
- Try to fit the data close to your area of interest (there are some limitations in the fit)



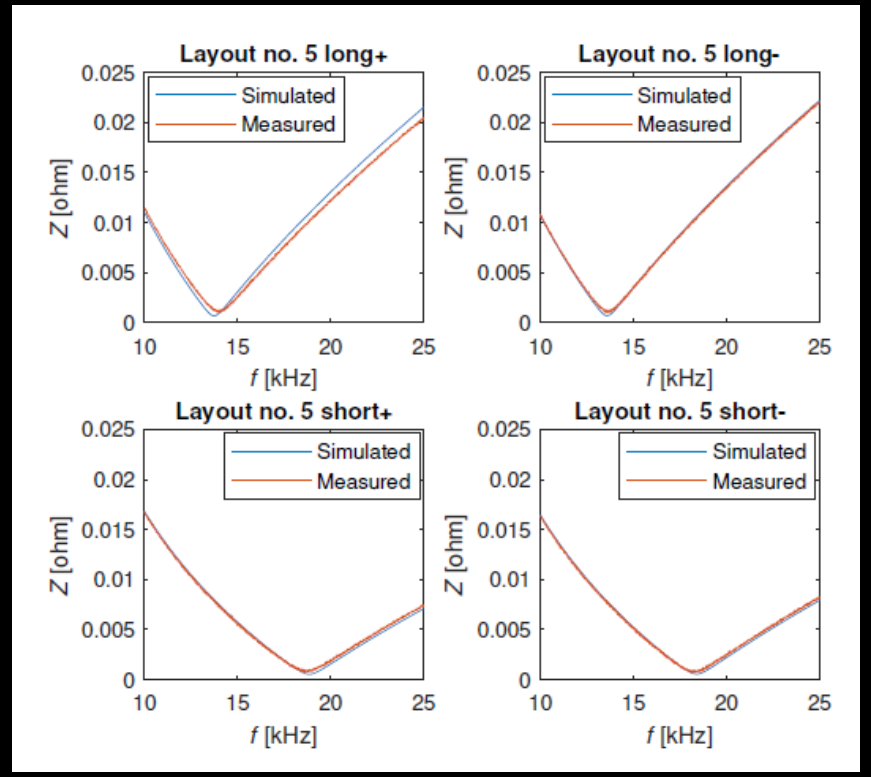
LABORATORY TEST SETUP

- Busbars of layout no. 5 were first measured using an impedance analyzer to measure the loop inductances
- Then a fully functional phase leg was built and tested to verify its switching characteristics
- Connecting strips were used in place of the IGBT modules to measure the impedance
- The FEM simulation was repeated with the connecting strips to get comparable results



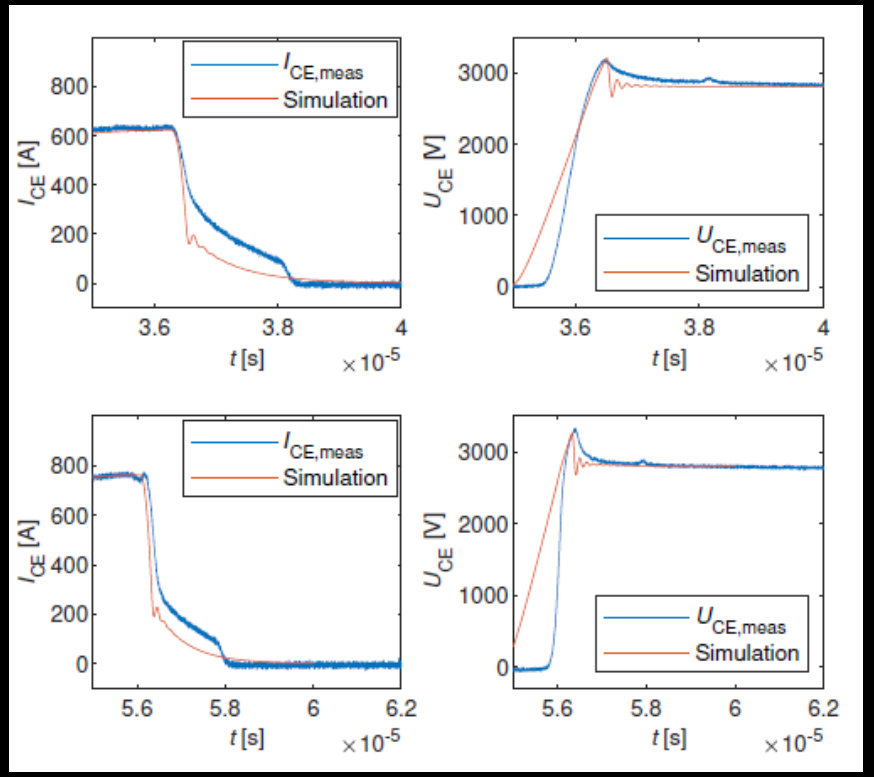
RESULTS

- The busbar impedance was found to have a good agreement with the simulation results verifying the model
- Only the long loop of DC+ shows some deviation that would result in small underestimation of the inductance value



RESULTS

- The switching waveforms of the IGBTs were found to have a good agreement with the simulation results considering the areas of interest
- Di/dt during turn-off has similar value although the tail current waveform shows the limitations of the semiconductor model
- Voltage du/dt is not accurate but the overshoot amplitudes are very similar in both cases



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THANK YOU !


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